LOW NOISE ELECTRONICS
FOR LIQUID ARGON DETECTORS

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FLARE WORKSHOP

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- Noise Fundamentals: Series, Parallel, 1/f noise sources
- Transmission line connection to the detector
- ICARUS case
- Cable skin effect losses
- Wire “diffusive line” noise
- Devices: GaAs, BJT, Si JFET, CMOS
- Considerations on Cryogenic Electronics
- Conclusions

Equivalent Noise Charge: ENC (S/N ratio)

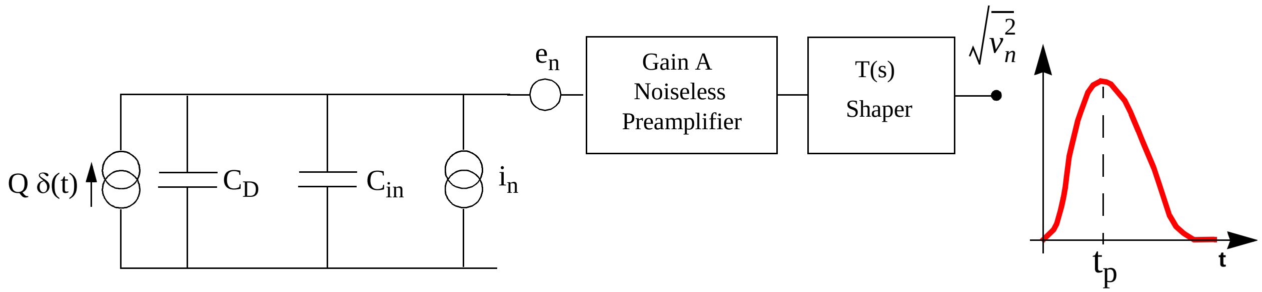
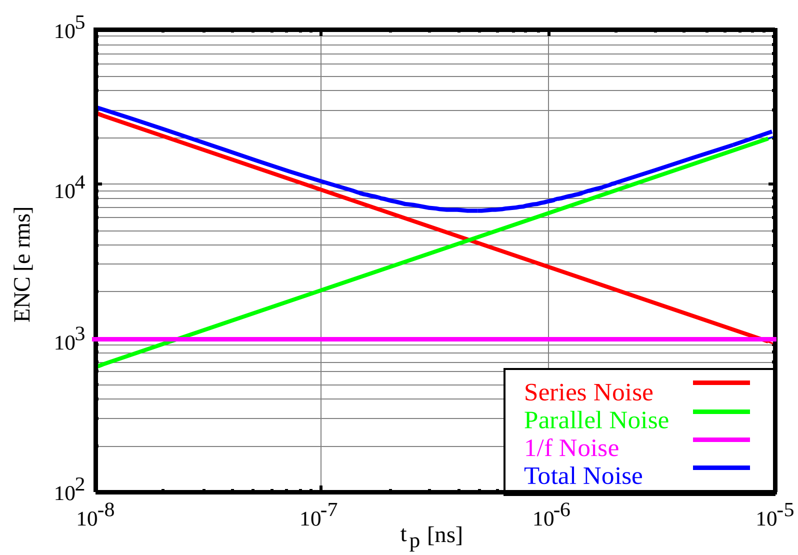


Figure 0-1.

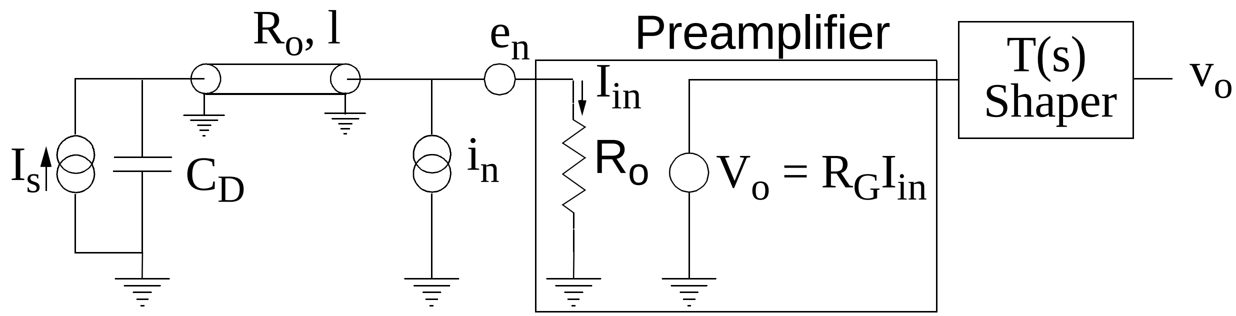
An infinitely narrow probability density function of the detector charge would appear at the output of the analog processing chain as a gaussian distribution with the variance $\sigma(e_n, i_n)$. This variance can be referred to the input as the *equivalent noise charge* (ENC), defined as the *current that delivered as an impulse at the preamplifier input will generate at the output a signal of amplitude σ.*

$$ENC = \frac{1}{q}\left(\frac{1}{2}\cdot e_n^2 \cdot C_T^2 \cdot \frac{A_S}{t_p} + \frac{1}{2}\cdot i_n^2 \cdot t_p \cdot A_P + C_{1/f}A_{1/f}\ C_T^2\right)^{(1/2)} \quad \text{(rms electrons)}$$

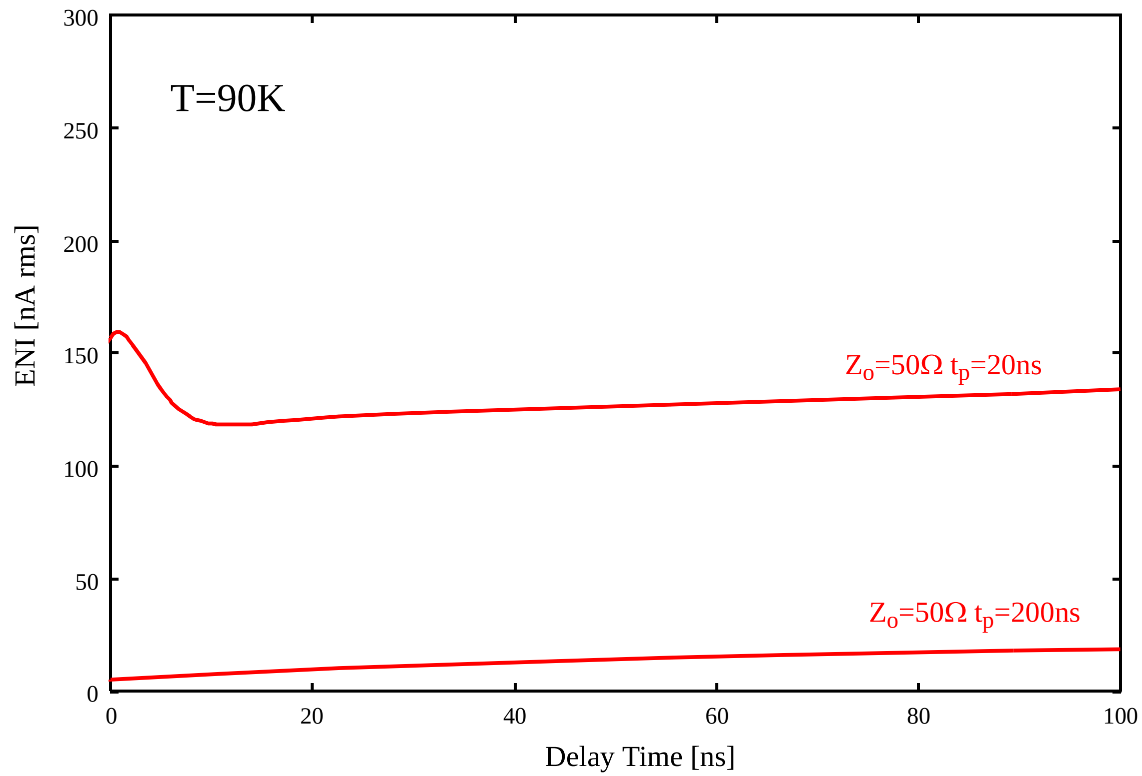


The parameters used are: $e_n = 0.5\ nV/\sqrt{Hz}$, $i_n = \sqrt{4K_BT/R_F}$, $C_{TOT} = 1nF$, $R_F = 1\ k\Omega$ and the filter is CR - RC^2.

Transmission Line Connection: Ideal Lossless Line

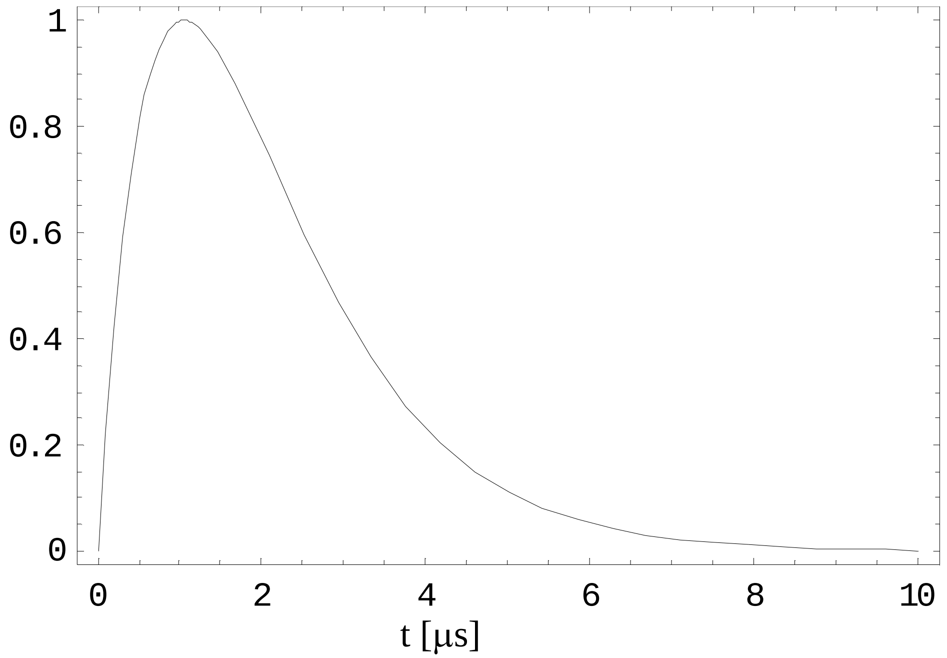


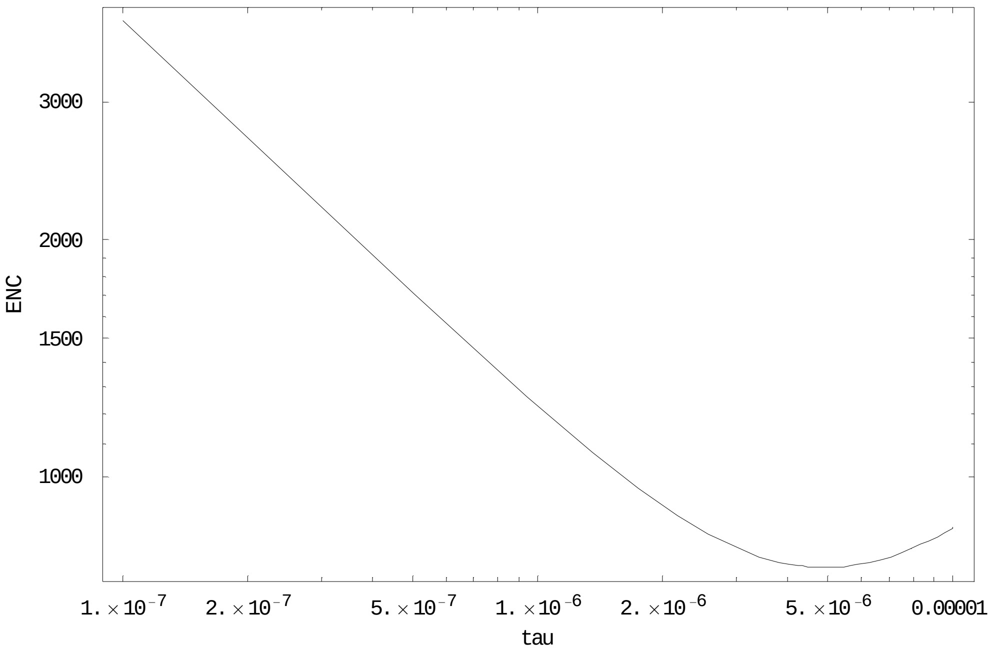
$$\overline{v^2_{on,s}} = \frac{e_n^2}{4R_0^2}\frac{1}{2\pi}\int_0^\infty \left|R_G(1+\Gamma e^{-2j\omega t_d})T(j\omega)\right|^2 d\omega \qquad \overline{v^2_{on,p}} = \frac{i_n^2}{4}\frac{1}{2\pi}\int_0^\infty \left|R_G(1-\Gamma e^{-2j\omega t_d})T(j\omega)\right|^2 d\omega$$



ICARUS CASE: ENC vs. shaping time

Assume a CR-RC shaping





- e_n = 0.4 nV/Sqrt[Hz] (slope 2.5e^-/pF)
- R_f = 1E6 Ω
- ENC = 500 e^- + 2.5 e^-/pF at 1 μs shaping time constant

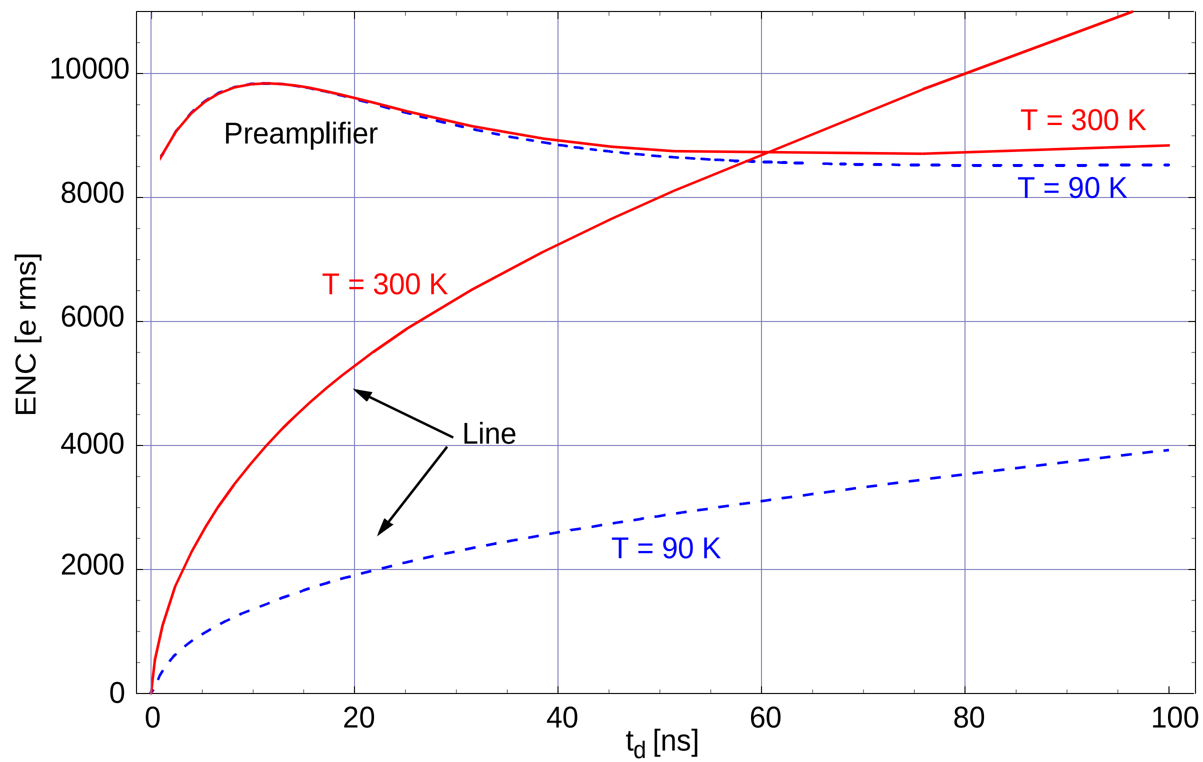
Other noise sources: Cable Skin Effect losses

Due to the skin effect at high frequency the conduction takes place only near the surface of a conductor, and the current density decays exponentially with depth. The distance at which it is reduced by 1/e is the penetration depth:

$$\delta = \left(\frac{2\rho}{\omega\mu}\right)^2$$

The skin effect penetration depth is 66 μm at 1 MHz for copper at 20 ^{o}C and 29 μm at 90 K. For a coaxial cable of inner radius a and outer radius b the resistance per unit length is:

$$R_{SC} = \frac{1}{2\pi}\left(\frac{1}{a} + \frac{1}{b}\right)\sqrt{\frac{\omega\mu\rho}{2}}$$

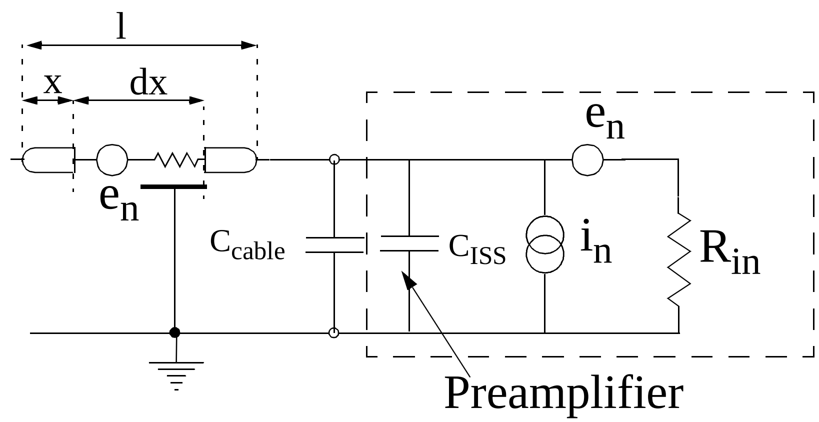


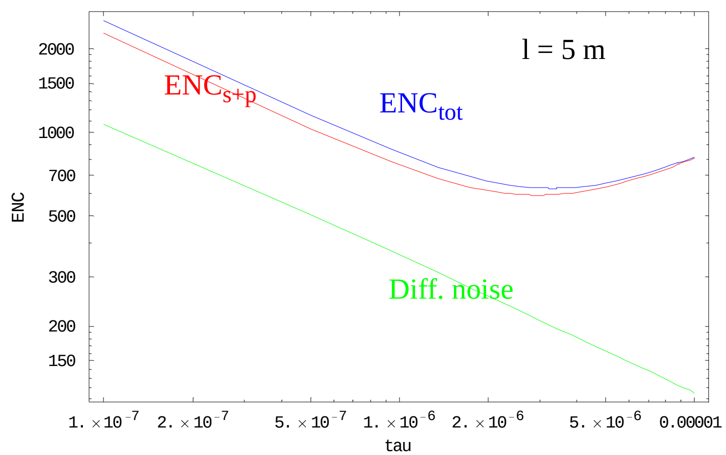
Calculation of different contributions to the equivalent noise charge. The values assumed are: $_n = 0.5\ nV/\sqrt{H}$, C_D = 400 pF, R_0 = 50 Ω and t_p = 20 ns, CR^2- RC^2 bipolar shaping. (a): The preamplifier noise contribution only, assuming the line at 300 K (solid line) and 90 K (dashed line) resulting in a different attenuation. (b): is the contribution of the noise generated by the distributed resistance of the line (“skin effect noise”) at 300 K (solid line) and 90 K (dashed line). The line skin effect resistance is R_S = 0.56 Ω at 10 MHz.

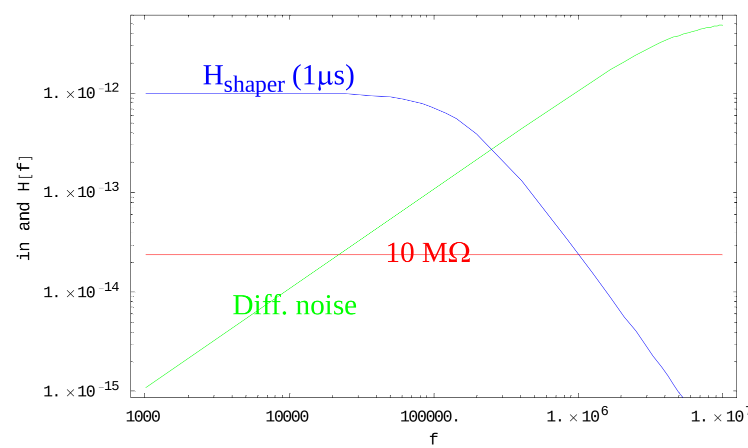
RECOMPUTE at 90 K find temperature coefficient of steel

Other Noise Sources: Wire "diffusive line" noise

The equivalent noise resistance of a low noise device with en = 0.4 nV/√Hz is only 10 Ω: any resistor in series with the input increases the noise. The stainless steel wire (ρ = 70 μΩ/cm at 20 ^{o}C) along with the capacitance to ground (i.e. "low impedance" nodes) constitutes an R-C diffusive line:







Noise current and ENC contribution of the wire diffusive line noise in comparison to the series and parallel noise. Wire length = 5m.

Devices: Gallium Arsenide

•High 1/f Noise, especially at room temperature

•Works at cryogenic temperature (better: lower series noise, lower 1/f noise)

•Expensive technology

•Limited availability: longer development time

•Used in the ATLAS Hadronic End-Cap calorimeter (developed by MPI Munich)

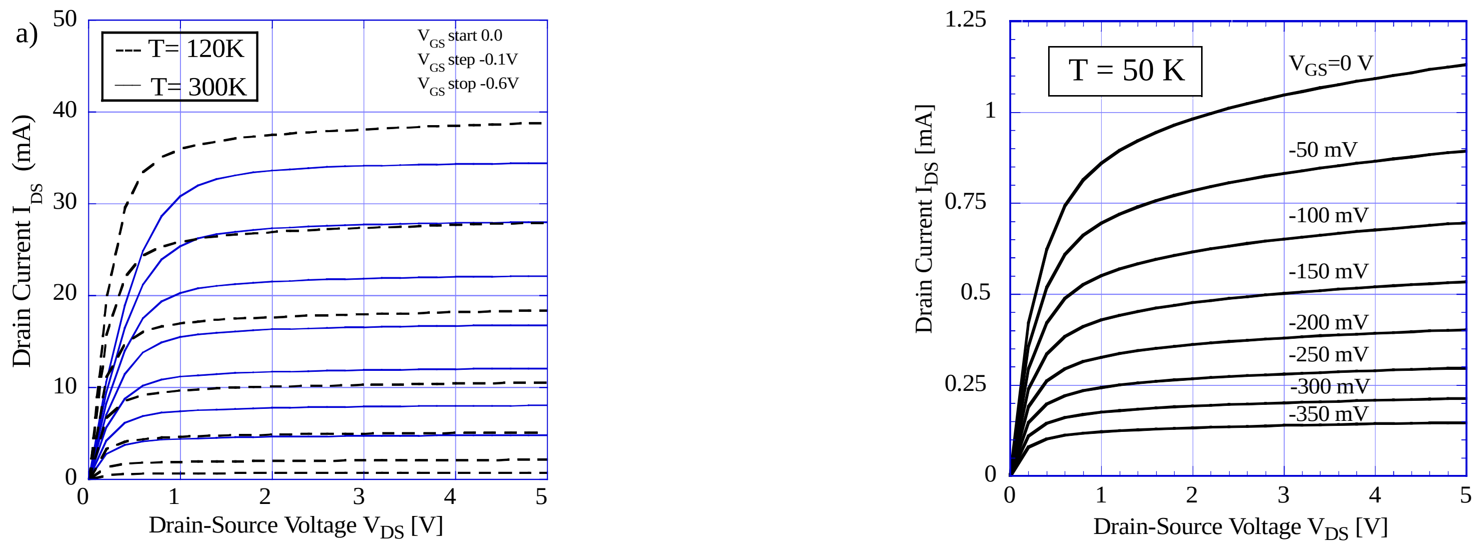
•Prototypes developed for ATLAS LAr at INFN Milano
(D. Camin et al.)

•**CONCLUSION:**

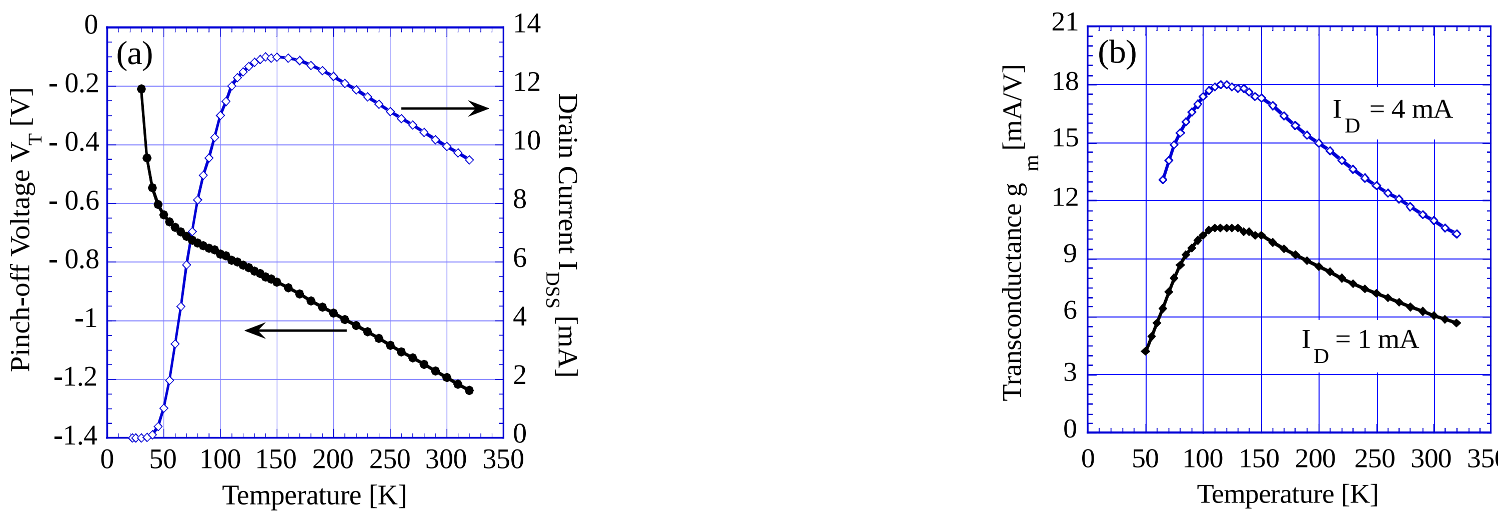
Probably not suitable for room temperature.

Could work at cryogenic temperature

Si JFET: Temperature Effects:

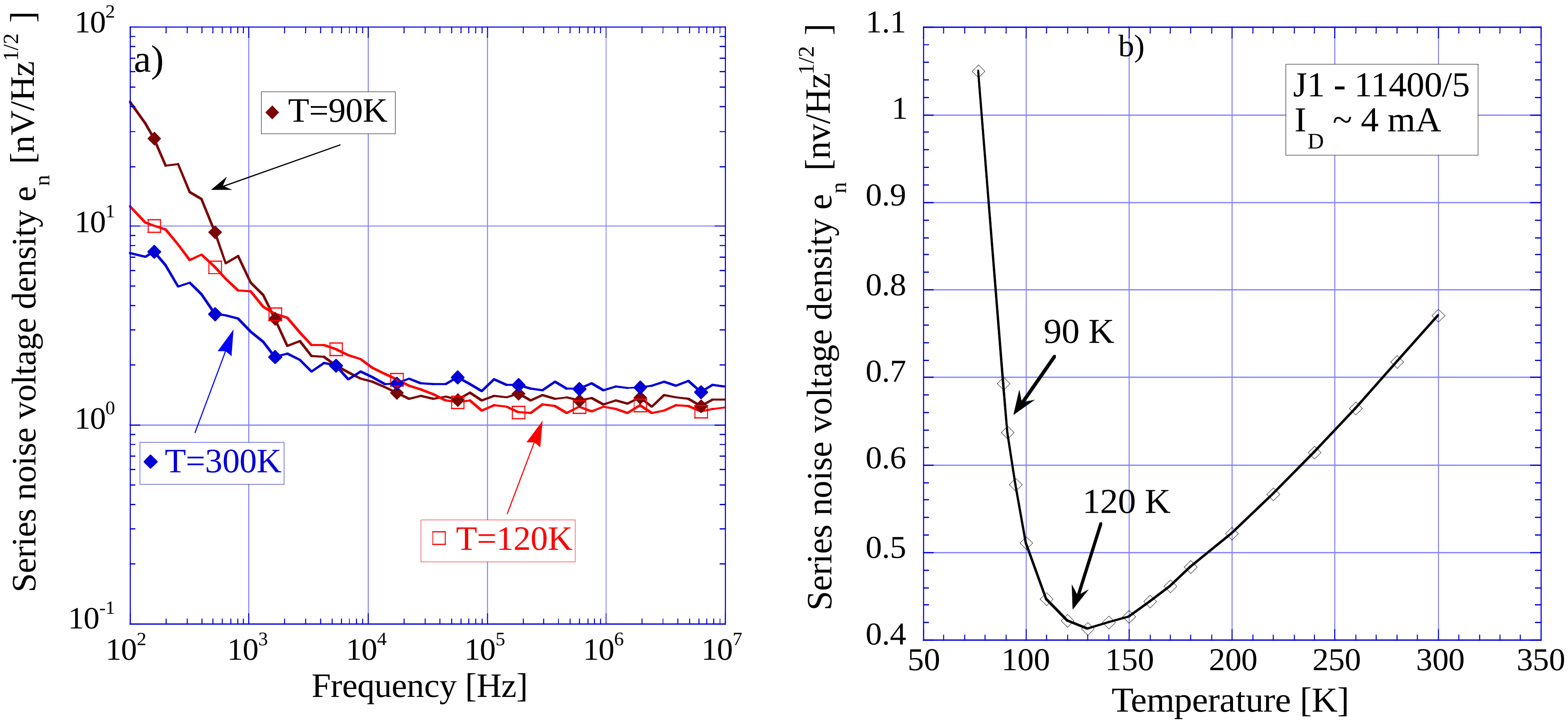


NJFET DC characteristics vs. temperature. (a): I_D vs. V_{DS} characteristics of a monolithic H-type (see text) NJFET transistor (W/L=11,400/5) at T = 120K (dashed line) and = 300 K (solid line). (b): I_D vs. V_{DS} characteristics at T = 50 K for a W/L = 2500/5 monolithic NJFET.



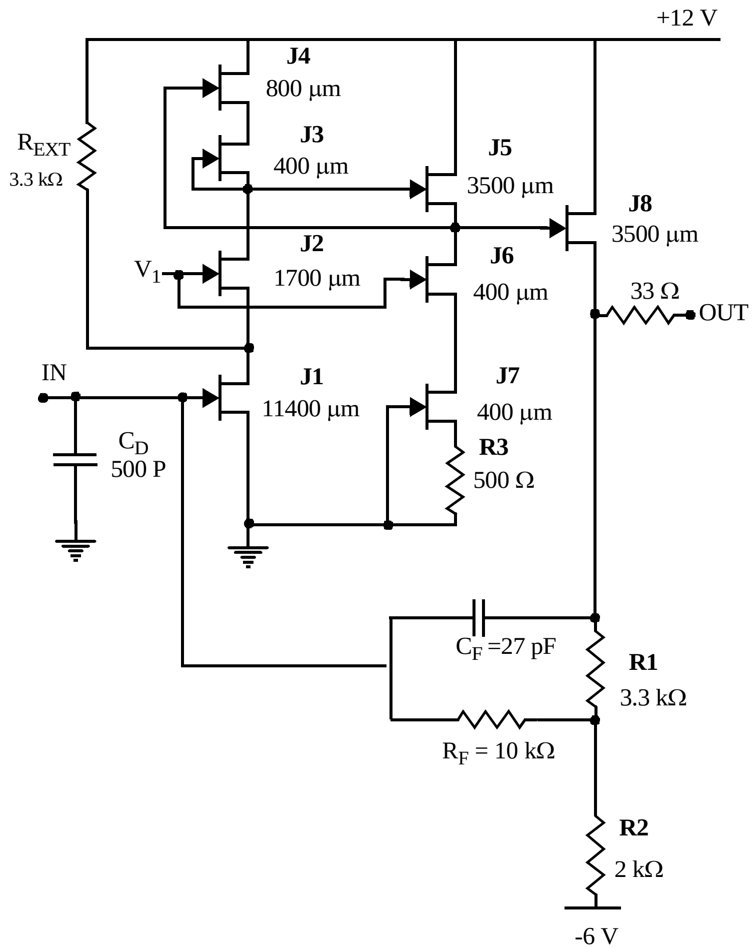
Temperature effects on the pinch-off voltage V_T and maximum current I_{DSS} (a) and on g_m (b) down to the freeze-out region. The measurement has been performed on a W/L=2500/5 device.

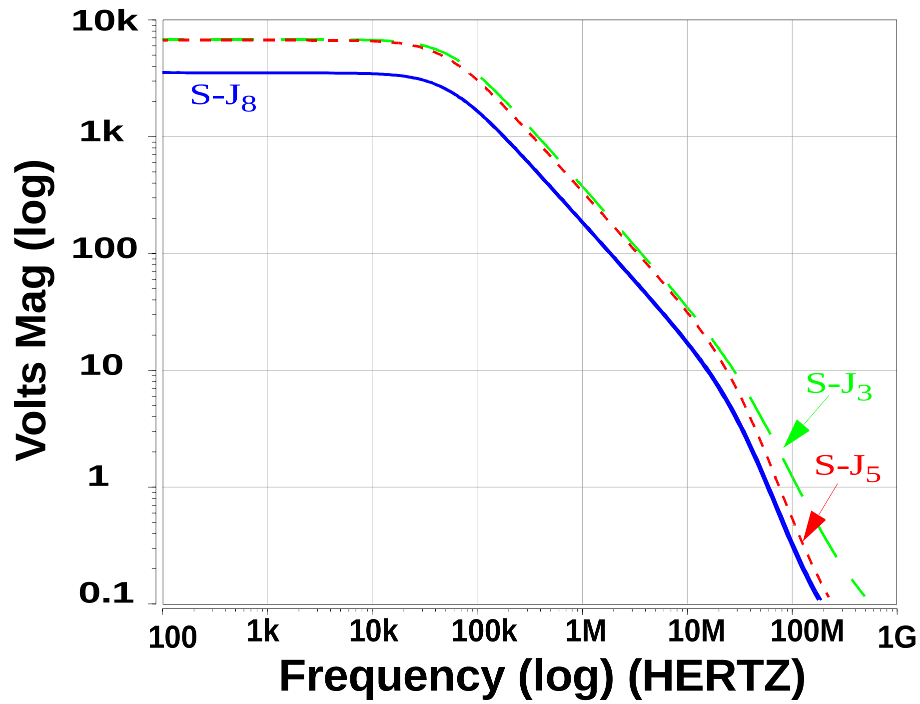
Si JFET: Noise vs. Temperature



Noise characteristics vs. temperature. (a): Series noise voltage density at 300 K, 120 K and 90 K for an unirradiated monolithic H-type NJFET (W/L = 2800/5). The transistor has been measured in the saturation region with V_{DS} = 2.5 V and I_D = 1 mA. (b): Temperature dependence for the high frequency component (white noise) of the series noise voltage density of a preamplifier whose input device is a monolithic H-type NJFET (W/L = 11400/5). The e_n values have been obtained from equivalent noise charge measurements. The input transistor was operating in the saturation region with a standing current I_D = 4 mA at room temperature.

JFET Monolithic Preamplifier



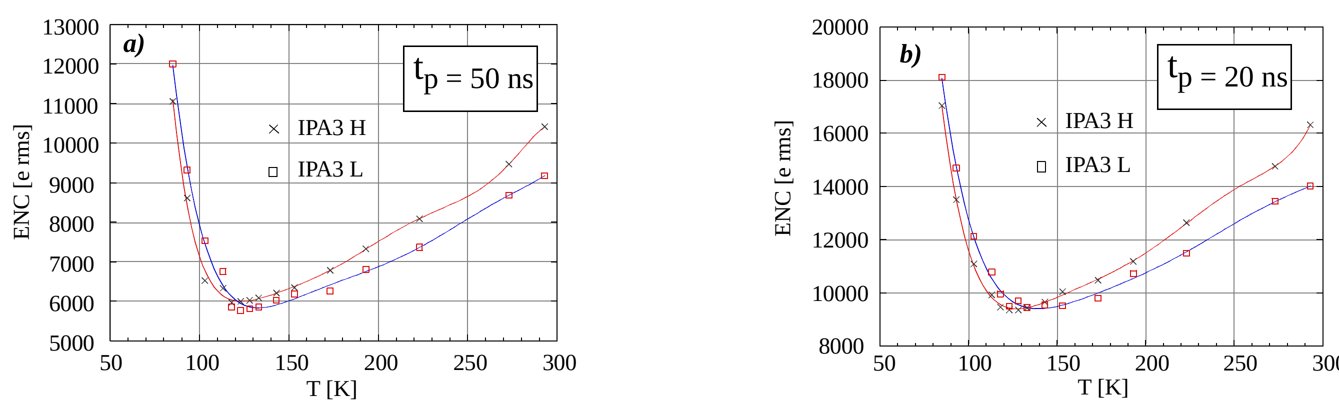


SPICE plot of the forward gain of the IPA3 preamplifier at various nodes. The input-output gain is the one measured on the source of J8.

Experimental Characterization

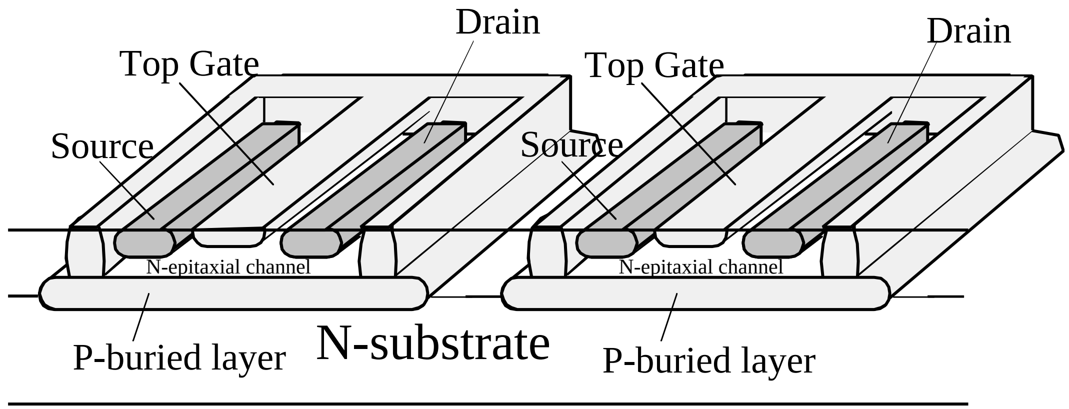
IPA3 measured characteristics

Parameter		L-type	H-type
Input Device		NJFET, W = 11400 μm, L = 5 μm	
Open-loop input capacitance		50 pF	40 pF
Power dissipation		80 mW	
DC gain A_0	Z_{OUT} = 10 kΩ	82 dB	75 dB
	Z_{OUT} = 100 Ω	76 dB	70 dB
Rise time (C_D = 500 p, C_F = 33 pF)		15 ns	
Noise voltage /√Hz] (f > 1 kHz)	T= 300 K	0.6	0.7
	T = 120 K	0.4	0.4
Equivalent noise charge [e rms] $(RC)^2$ -$(CR)^2$ bipolar shaping at t_p = 50 ns		$ENC = 1200 + 18\,C_D$	$ENC = 1100 + 21\,C_D$



ENC as a function of temperature for IPA3 L and H preamplifiers.The measurements have been carried out with C_D = 500 pF detector capacitance and bipolar shaping obtained from an (RC)2 -(CR)2 filter.
a): 50 ns peaking time; b): 20 ns peaking time.

DEVICES: Silicon JFET: Monolithic JFET Process

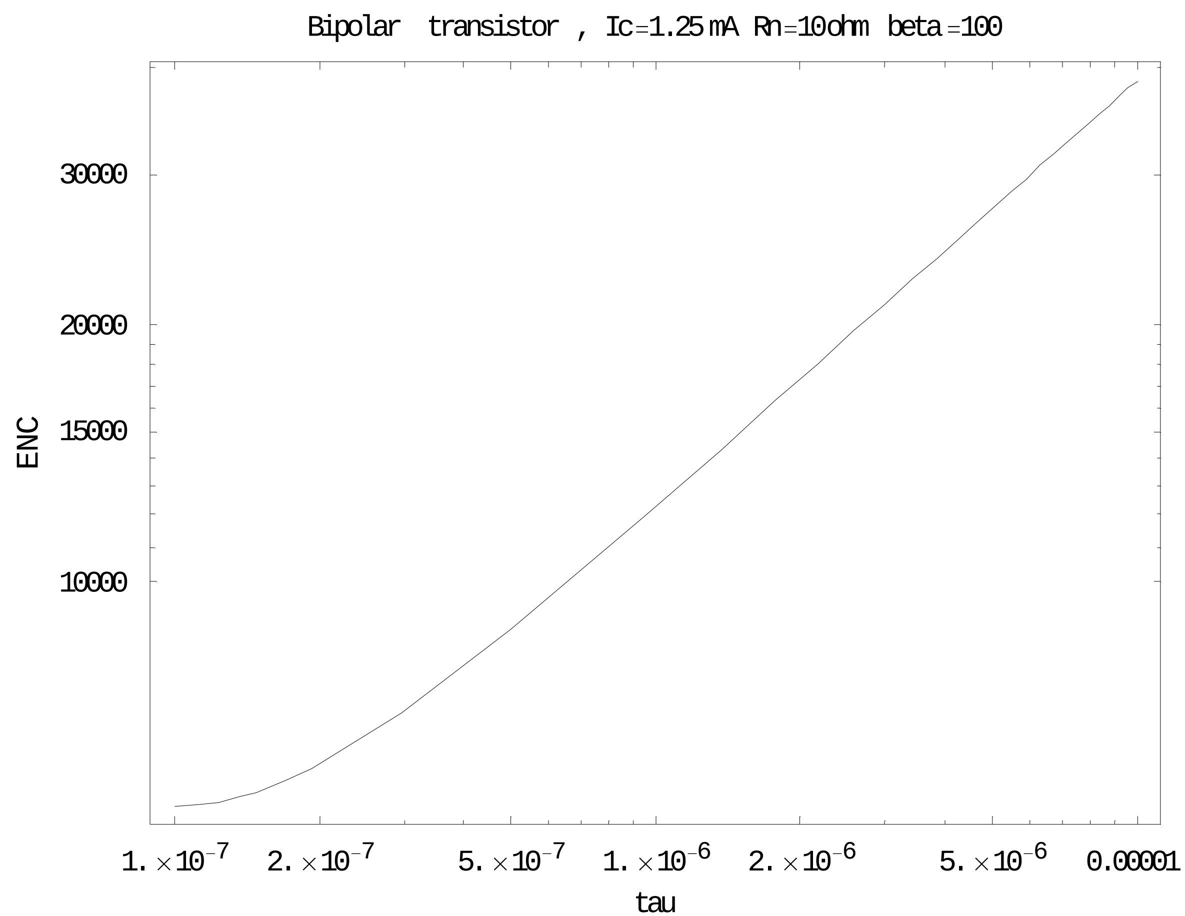


Cross section of adjacent devices built by means of the buried layer process.

Simplified Fabrication Process (Buried Layer, Diffused S, D, G Process)

1	Starting wafer: 0.5 Ωcm, N-type, (111) Silicon
2	Diffuse back-gate wells: 0.002 Ωcm
3	Grow oxide: t_{ox} ~ 50 nm
4	Strip oxide, chemical clean and epi-growth. t_{epi} ~ 5-7 μm R_{epi} = 0.5 Ωcm (L-type) and 1.5 Ωcm (H-type)
5	Pattern and diffuse isolation ring (P-type)
6	Pattern gate and gate diffusion (P-type)
7	Pattern source and drain and diffusion (N-type)
8	Open contact window. Probe test structures. Gate targeting (by additional drive-in)
9	Nitride deposition (dielectric layer to isolate metal)
10	Evaporate and pattern metal (aluminum)
11	Nitride protective overcoat

Devices: Bipolar Transistors



- The I_b = 12.5 μA, corresponding to R_{par} = 4000 Ω.
  The noise corner time constant is

$$\tau_C = C_d\sqrt{R_s R_p} = 100 ns$$

- In short: forget it.
- Even using SiGe (β = 500-1000 at cryogenic temperature) is unfeasible

Devices: CMOS

PMOS TMSC 0.25 μm Technology

L = 0.36 μm W = optimized for minimum noise at a given power (PMOS, L=0.36μm, W=42mm, Cg=91pF, gm=153mS @ 20mW)

C_d = 500 pF t = 1 μs

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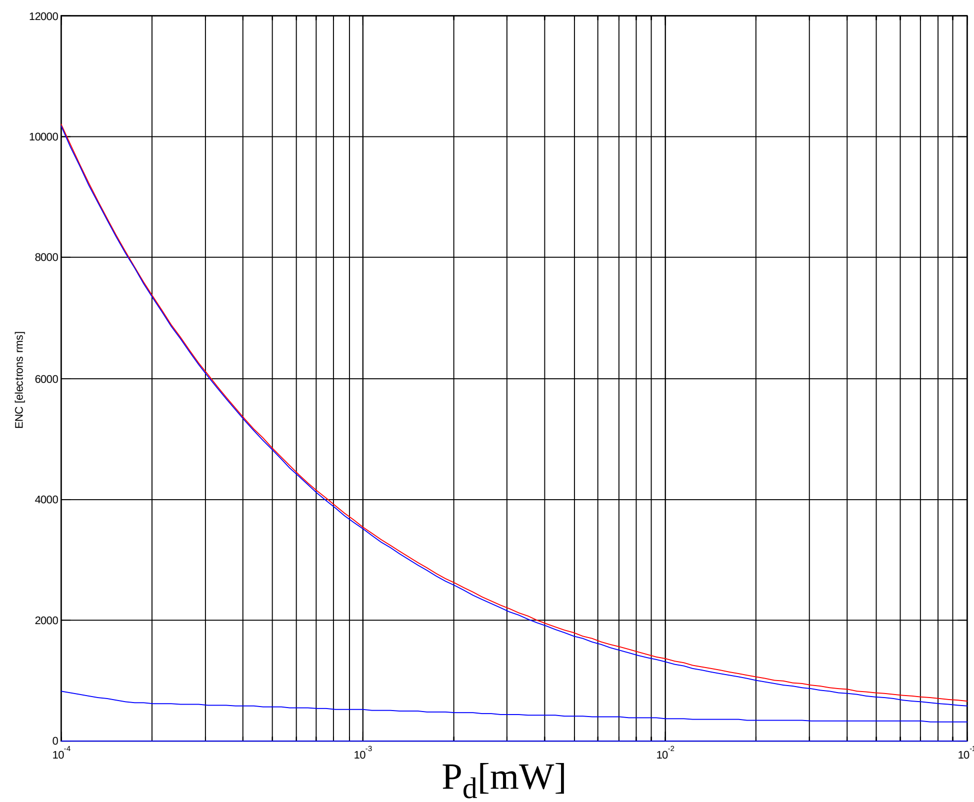

Needs Id = 10 mA (P = 20mW) to reach ENC < 1000 e at 1 μs

From G. De Geronomo

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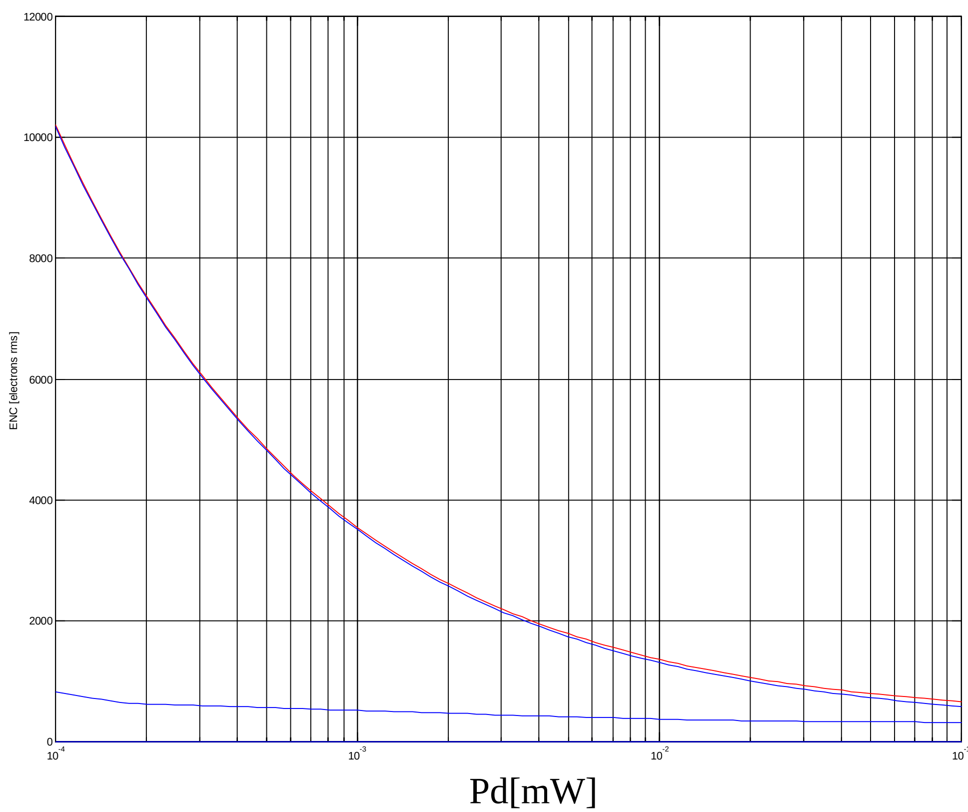
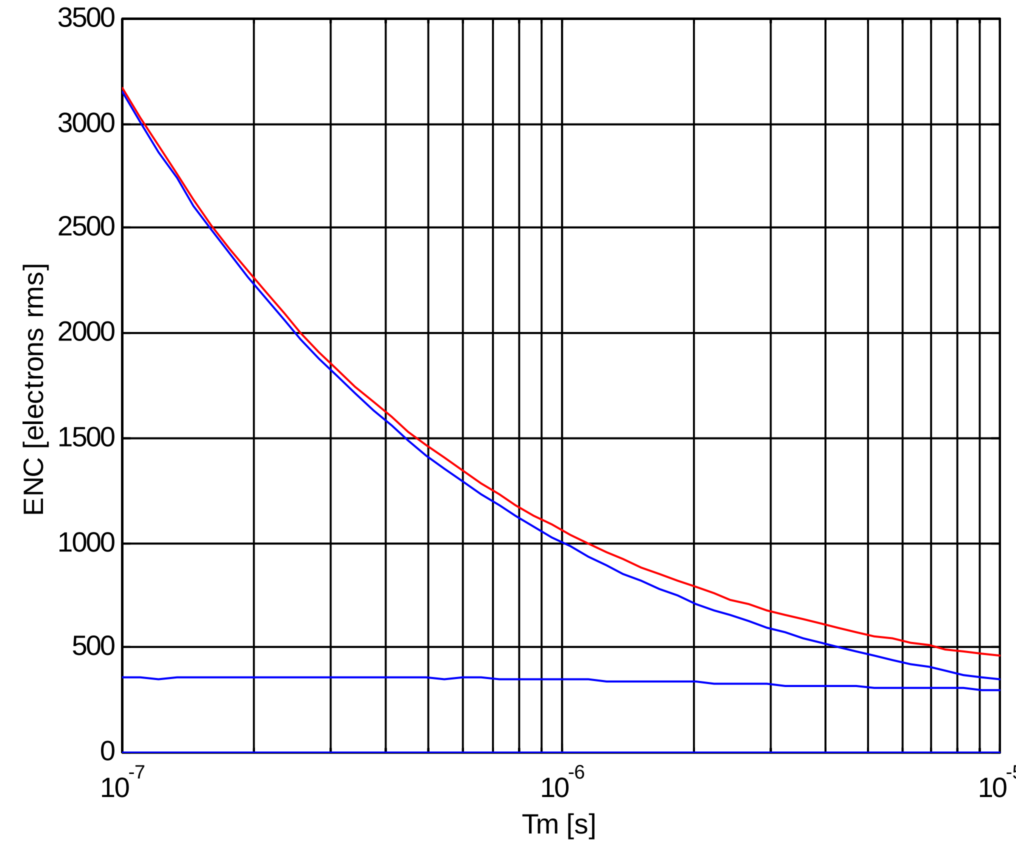




Needs Id = 10 mA (P = 20mW) to reach ENC < 1000 e at 1 µs

P = 20 mW Cd = 500 pF vs. measurement time

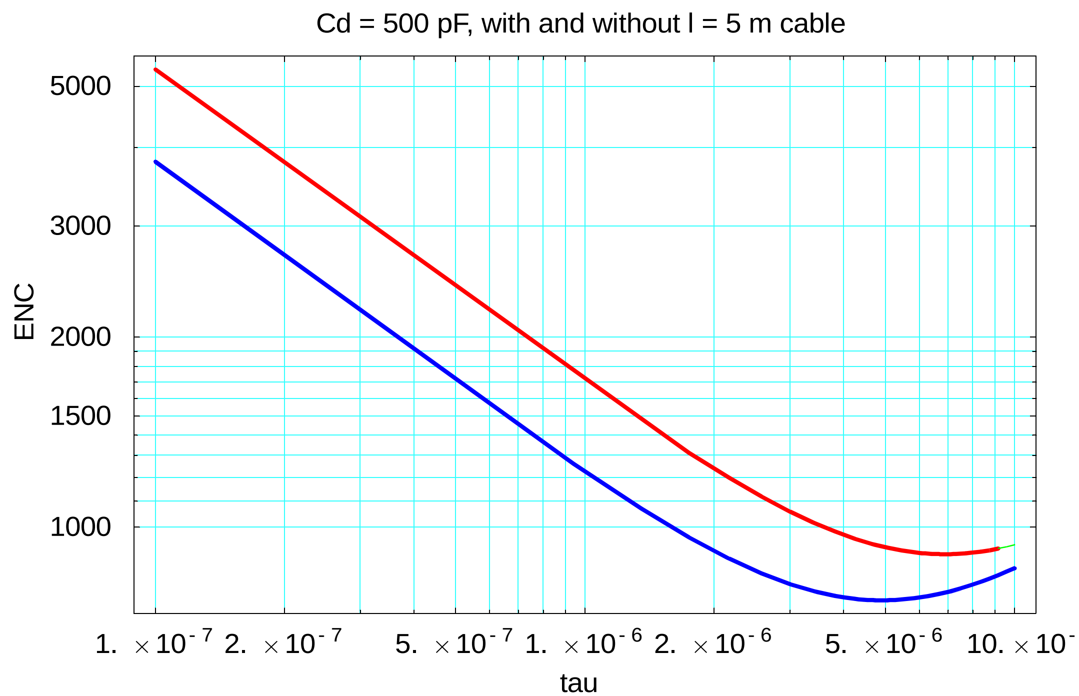
(From G. De Geronimo)

Reference: "**MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers",** G. De Geronimo, P. O'Connor, presented at the "2004 IEEE Nuclear Science Symposium", Rome

Cryogenic vs. "Warm" Electronics

- Cable capacitance ~50pF/m $\Rightarrow$ 200 pF for 4 m cable run (500 pF for 10 m)
- Cd ~ 500 pF $\Rightarrow$ 700 pF total capacitance contributing to the noise (1000 pF for 10 m)

CRYOGENIC ELECTRONICS REDUCES THE NOISE



OTHER ADVANTAGES:

- Avoids transmission of very low level signals (better "Faraday cage")
- at the cost of complicating the electronics (MORE POWER!), could reduce the number of feedthrough by data reduction ("sparsification") in hardware
- reliability (if properly designed and built)

DISADVANTAGES

- Bubbling
- cryogenic load
- Purity